



10-5-01 0309 #3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Saputro, Stephanus D.; Zhang, Lan  
Assignee: Dell Products, L.P.  
Title: Reducing Inductance Of A Capacitor  
Serial No.: 09/905,474 Filing Date: July 13, 2001  
Examiner: Not Assigned Group Art Unit: Not Assigned  
Docket No.: M-11685 US

San Jose, California  
October 4, 2001

COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or

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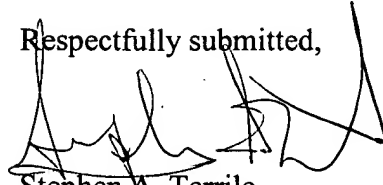
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3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

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Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-11685 US		09/905,474	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Saputro, Stephanus D.; Zhang, Lan			
					Filing Date		Group	
					July 13, 2001			
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	David A. Baranauskas and Douglas E. Wallace, Jr., "Capacitive Structure for Via Impedance Tuning"; September 14, 1999, Serial No. 09/395,788. <i>361/793 Au 2841</i>						
	AR	Doreen S. Fisher and Thad McMillian, "Printed Circuit Assembly Having Conductive Pad Array With In-Line Via Placement", June 28, 2000, Serial No. 09/605,905. <i>361/777 Au 2841</i>						
	AS							
Examiner			Date Considered					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								